Claims

[c1] What is claimed is:

1.A bipolar junction transistor (BJT) comprising:

a substrate;

a dielectric layer formed on a predetermined region of the substrate;

an opening formed in the dielectric layer, and a portion of the substrate being exposed;

a heavily doped polysilicon layer formed on a sidewall of the opening to define a self-aligned base region in the opening;

an intrinsic base doped region formed within the substrate and in a bottom of the opening by implanting through the self-aligned base region;

a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled with the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region.

[c2] 2.The bipolar junction transistor of claim 1 wherein the heavily doped polysilicon layer is doped with a boron dopant with a dosage ranging from 1E19 to 1E21 atoms/cm^3.

[c3] 3.The bipolar junction transistor of claim 1 wherein the substrate is a silicon substrate.

[c4] 4.The bipolar junction transistor of claim 1 wherein the substrate is a non-selective epitaxial silicon substrate.

[c5] 5.The bipolar junction transistor of claim 1 further comprising a self-aligned silicide (salicide) layer formed on the emitter conductivity layer.

[c6] 6.The bipolar junction transistor of claim 1 further comprising a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

[c7] 7.The bipolar junction transistor of claim 1 further comprising an extended conductivity layer formed on the dielectric layer electrically connected to the

heavily doped polysilicon layer.

[c8] 8.The bipolar junction transistor of claim 7 further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

[c9] 9.The bipolar junction transistor of claim 7 wherein the extended conductivity layer is composed of in-situ doped polysilicon.

[c10] 10.The bipolar junction transistor of claim 1 wherein the dielectric layer is a shallow isolation trench (STI) oxide layer, and the predetermined region is a STI region.

[c11] 11.A hetero-junction bipolar junction transistor (HBT) comprising:
a substrate;
a dielectric layer formed on a predetermined region of the substrate;
an opening formed in the dielectric layer, and a portion of the substrate being exposed;
a SiGe epitaxial layer formed on a sidewall and a bottom of the opening;
a spacer formed on the SiGe epitaxial layer to define a self-aligned emitter region in the opening; and
an emitter conductivity layer being filled with the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the SiGe epitaxial layer.

[c12] 12.The hetero-junction bipolar junction transistor of claim 11 wherein the substrate is a silicon substrate.

[c13] 13.The hetero-junction bipolar junction transistor of claim 11 wherein the substrate is a non-selective epitaxial silicon substrate.

[c14] 14.The hetero-junction bipolar junction transistorof claim 11 further comprising a self-aligned silicide (salicide) layer formed on the emitter conductivity layer.

[c15] 15.The hetero-junction bipolar junction transistor of claim 11further comprising a selective implant collector (SIC) region formed in the substrate

beneath the SiGe epitaxial layer.

[c16] 16.The hetero-junction bipolar junction transistor of claim 11 wherein the SiGe epitaxial layer extends outside the opening and above the dielectric layer.

[c17] 17.The hetero-junction bipolar junction transistor of claim 11 wherein the dielectric layer is a shallow isolation trench (STI) oxide layer, and the predetermined region is a STI region.